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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,285	07/14/2003	Robert C. Pack	CA7010492001	7734

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,285	PACK ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/620285 filed on 06/24/03.

Claims 1-36 remain pending in the application.

Response to Arguments

Applicant's arguments with respect to claims 1-36 have been considered and are Persuasive. However, new grounds of rejection are introduced below.

Specification

The disclosure is objected to because of the following informalities: In paragraph [00183] needs to insertion of serial number. Appropriate correction is required.

Drawings

The drawings are objected to because Fig 1 should be labeled Prior Art. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanian et al. (U.S Patent 6579651).

3. As to claims 1, and 22 Subramanian et al. teach a method for writing a mask, comprising: generating integrated circuit design data (fig 5a-5d fig 10-14 element 100 and element 635 col 8 lines 1-3 and col 12 lines 20-30); and using information for interfeature relationships of the integrated circuit design data to write the mask without the use of tags (see fig 5a –5d element 80 mask writer col 7 lines 64 to col9 lines 39).

4. As to claim 2, and 23 Subramanian et al. teach wherein the interfeature relationships are on one layer of the integrated circuit design (see col 1 lines 37-col 2 lines 56).

5. As to claim 3, and 24 Subramanian et al. teach wherein the interfeature relationships am across multiple layers of the integrated circuit design (see col 1 lines 37-col 2 lines 56).

6. As to claim 4, and 25 Subramanian et al. teach wherein the interfeature relationships comprise: interfeature process proximity effects; interfeature coupling across layers (see col 1 lines 37-col 2 lines 56); interfeature electronic relationships (see col 1 lines 37-col 2 lines 56 and

summary); or wire interconnects longer than a given length (see col 1 lines 37-col 2 lines 56 and summary).

7. As to claim 5, and 26 Subramanian et al. teach wherein using the information for interfeature relationships to write the mask further comprises: passing the information for interfeature relationships to a mask writing system mask (see fig 5a –5d element 80 mask writer col 7 lines 64 to col9 lines 39).

8. As to claim 6, and 27 Subramanian et al. teach a method for generating a lithography mask or a printed wafer, comprising: generating integrated circuit design data (fig 5a-5d fig 10-14 element 100 and element 635 col 8 lines 1-3 and col 12 lines 20-30); analyzing the integrated circuit design data to generate context information for each feature without the use of tags (see fig 5a –5d element 80 mask writer col 7 lines 64 to col9 lines 39); and using the context information to write each feature of the mask or printed wafer (see fig 5a –5d element 80 mask writer col 7 lines 64 to col9 lines 39).

9. As to claim 7, and 28 Subramanian et al. teach wherein using context information comprises: analyzing mask features for contextual priority (see col 1 lines 37-col 2 lines 56 and summary).

10. As to claim 8, and 29 Subramanian et al. teach wherein using context information comprises: assigning priorities to the mask features (see fig 5a –5d element 80 mask writer col 7 lines 64 to col9 lines 39).

11. As to claim 9, and 30 Subramanian et al. teach wherein assigning priorities to the mask features comprises: applying criteria to mask design data by manual process (see fig 5a –5d element 80 mask writer col 7 lines 64 to col9 lines 39).

12. As to claim 10, and 31 Subramanian et al. teach wherein assigning priorities to the mask features comprises: applying criteria to mask design data by computer-aided automated process (see col 1 lines 37-col 2 lines 56).

13. As to claim 11, and 32 Subramanian et al. teach wherein using context information comprising: analyzing mask features to determine the circuit element expected to be produced by a lithography system at a chip wafer surface (see fig 5a –5d element 80 mask writer col 1 lines 29-62 col 7 lines 64 to col9 lines 39).

14. As to claim 12, and 33 Subramanian et al. teach further comprising: configuring a mask design database to include additional contextual mask design data generated in using the contextual information from the integrated circuit design data (see col 8 lines 15 to col 9 lines 38).

15. As to claim 13, and 34 Subramanian et al. teach further comprising: configuring the mask design database to optimize an order of mask design data for use by a mask writing system (see col 8 lines 15 to col 9 lines 38).

16. As to claim 14, and 35 Subramanian et al. teach wherein using context information comprises: passing context information to a mask writing system (see col 8 lines 15 to col 9 lines 38).

17. As to claim 15, and 36 Subramanian et al. teach wherein using context information comprises: controlling a mask writing system base on the context information (see col 8 lines 15 to col 9 lines 38).

18. As to claim 16, Subramanian et al. teach an apparatus for mask writing comprising: means for generating a design of an integrated circuit design (see fig 5a-5d fig 10-14 element

100 and element 635 col 8 lines 1-3 and col 12 lines 20-30); means for producing circuit contextual information for the integrated circuit design (see fig 5a-5d fig 10-14 element 100 and element 635 col 8 lines 1-3 and col 12 lines 20-30); means for capturing the circuit contextual information in a mask design database (see col 8 lines 15 to col 9 lines 38); mean for producing mask contextual information for mask elements in the mask design database based on the circuit contextual information (see col 8 lines 15 to col 9 lines 38 and background and summary); means for configuring the mask design database to reflect the mask contextual information (see fig 5a – 5d element 80 mask writer col 7 lines 64 to col 9 lines 39); and means for writing the mask elements on a mask substrate (see fig 5a –5d element 80 mask writer col 7 lines 64 to col 9 lines 39).

19. As to claim 17, Subramanian et al. teach wherein said means for writing further comprises: means for determining manufacturing enhancements for one or more mask elements based on the mask contextual information (see col 1 lines 37-col 2 lines 56); and means for applying the manufacturing enhancement to the mask element (see col 1 lines 37-col 2 lines 56).

20. As to claim 18, Subramanian et al. teach further comprising: means for producing priority information for the mask elements based on features of the ask elements (see fig 5a –5d element 80 mask writer col 7 lines 64 to col 9 lines 39).

21. As to claim 19, Subramanian et al. teach a method for mask writing, comprising: designing an integrated circuit; passing the design data to a context and priority analysis step (see fig 5a-5d fig 10-14 col 8 lines 1-3 and col 12 lines 20-30); analyzing design data for each mask element to determine a circuit function, circuit criticality context, and priority for each mask element (see col 8 lines 15 to col 9 lines 38 and background and summary); including the circuit

function, circuit criticality context, and priority data in a mask design data file (see col 8 lines 15 to col 9 lines 38 and background and summary); and using the mask design data file to write a mask (see fig 5a –5d element 80 mask writer col 7 lines 64 to col 9 lines 39).

22. As to claim 20, Subramanian et al. teach wherein design data from the integrated circuit design comprises: polygonal shape, location, layout geography, circuit functionality and circuit criticality data for each mask element (see col 1 lines 37-col 2 lines 56).

23. As to claim 21, Subramanian et al. teach wherein analyzing further comprises: comparing design data for each mask element to design data for other mask elements and to a predetermined set of mask criteria (see col 1 lines 37-col 2 lines 56).

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
April 16, 2005

A. M. Thompson
Primary Examiner
Technology Center 2800